WHAT IS CLAIMED IS:

1. A circuit for calculating reciprocal values, comprising:

an input for receiving input data, the input data being partitionable into a plurality of segments including a first segment and a second segment;

a first look-up table coupled to the input, the first look-up table having stored therein first pre-calculated values, the first look-up table configured to receive the first segment and for providing a first respective one of the first pre-calculated values in response to the first segment;

a first shifter circuit coupled to the first look-up table, the first shifter circuit configured to receive the first respective one of the first pre-calculated values and for generating a first shifted value by shifting the first respective one of the first pre-calculated values according to a relative position of the first segment within the input data;

a second look-up table coupled to the input, the second look-up table having stored therein second pre-calculated values, the second look-up table configured to receive the second segment and for providing a second respective one of the second pre-calculated values in response to the second segment;

a second shifter circuit coupled to the second look-up table, the second shifter circuit configured to receive the second respective one of the second pre-calculated values and for generating a second shifted value by shifting the second respective one of the second pre-calculated values according to a relative position of the second segment within the input data; and

an output selector circuit for selecting one of the first shifted value and the second shifted value as an approximate reciprocal value of the input data.

2. The circuit of claim 1, wherein the first and second pre-calculated values comprise approximate reciprocal values of addresses of the look-up table.

3. The circuit of claim 1, wherein the output selector circuit is configured to select the first shifted value provided the first shifted value is non-zero, and for selecting the second shifted value provided the first shifted value is zero.

4. A circuit for calculating reciprocal values, comprising:

an input for receiving input data, the input data being partitionable into a plurality of segments;

a selector circuit for selecting one of the segments;

a look-up table coupled to the selector circuit for receiving the selected segment, the look-up table having stored therein pre-calculated values, the look-up table configured to provide a respective one of the pre-calculated values in response to the selected segment; and

a shifter circuit coupled to the look-up table, the shifter circuit configured to shift the respective one of the pre-calculated values according to a relative position of the selected segment within the input data to generate an approximate reciprocal value for the input data.

5. The circuit of claim 4, wherein the selector circuit is configured to select a non-zero segment of the input data to be provided to the look-up table.

6. The circuit of claim 4 further comprising a first 2's complement circuit for converting a negative input data into the input data.

7. The circuit of claim 6 further comprising a second 2's complement circuit for converting the approximate reciprocal value into a negative approximate reciprocal value.

8. A method of calculating reciprocal values, comprising:

storing a plurality of reciprocal values in a look-up table in association with a plurality of possible input values;

receiving an input value, the input value having a larger bit-width than each of the possible input values;

partitioning the input value into a plurality of segments each having a bit-width corresponding to each of the possible input values;

selecting one of the segments and providing the selected one of the segments to the look-up table to retrieve a respective one of the reciprocal values; and

shifting the respective one of the reciprocal values according to a position of the selected one of the segments in relation to the input value to generate an approximate reciprocal value for the input data.

9. The method of claim 8, wherein the storing comprises:

storing the plurality of possible input values as indices of the look up table.

10. The method of claim 8, wherein the storing comprises storing the plurality of reciprocal values in a memory unit of a programmable logic device, wherein the plurality of input values comprise addresses of the memory unit.

11. A circuit for performing normalized least-mean-squared calculations, comprising:

an input for receiving a μ-Law encoded data value; and

a look-up table coupled to the input, the look-up table having stored therein a plurality of pre-calculated intermediate data values, the pre-calculated intermediate data values being operands for normalized least- mean-squared calculations, wherein the look-up table is configured to provide a corresponding one of the pre-calculated intermediate data values in response to the μ-Law encoded data value.

12. The circuit of claim 11, wherein the plurality of pre-calculated intermediate data values comprise a plurality of pre-calculated μ-Law expansion values.

13. The circuit of claim 11, wherein the look-up table stores a plurality of possible input values associated with the plurality of pre-calculated intermediate data values.

14. The circuit of claim 13, wherein the look-up table uses the plurality of possible input values as indices.

15. A circuit for performing normalized least-mean-squared calculations, comprising:

an input for receiving an A-Law encoded data value; and

a look-up table coupled to the input, the look-up table having stored therein a plurality of pre-calculated intermediate data values, the pre-calculated intermediate data values being operands of normalized least-mean-squared calculations, wherein the look-up table is configured to provide a corresponding one of the pre-calculated intermediate values in response to the A-Law encoded data value.

16. The circuit of claim 15, wherein the plurality of pre-calculated intermediate data values comprise a plurality of pre-calculated A-Law expansion values.

17. The circuit of claim 15, wherein the look-up table stores a plurality of possible input values associated with the plurality of pre-calculated intermediate data values.

18. The circuit of claim 17, wherein the look-up table uses the plurality of possible input values as indices.

19. A method of performing normalized least-mean-squared calculations, the method comprising:

receiving an input data, the input data comprising a μ-Law encoded data value; and

using the input data as an index to retrieve a pre-calculated intermediate data value from a look-up table, the look-up table having stored therein a plurality of pre-calculated intermediate values, wherein the pre-calculated intermediate data values comprise operands for normalized least- mean-squared calculations and correspond to a pre-determined range of μ-Law encoded data values.

20. The method of claim 19, wherein the plurality of pre-calculated intermediate values comprise a plurality of pre-calculated μ-Law expansion values.

21. A method of performing normalized least-mean-squared calculations, the method comprising:

receiving a A-Law encoded data value; and

using the A-Law encoded data value as an index to retrieve a pre-calculated intermediate data value from a look-up table, the look-up table having stored therein a plurality of pre-calculated intermediate values, wherein the pre-calculated intermediate data values comprise operands for normalized least- mean-squared calculations and correspond to a pre-determined range of A-Law encoded data values.

22. The method of claim 21, wherein the plurality of pre-calculated intermediate values comprise a plurality of pre-calculated A-Law expansion values.

23. In a programmable logic device, a circuit for determining a mathematical function for an input value, the circuit comprising:

an input for receiving the input value;

a look-up table coupled to the input for receiving the input value, the look-up table comprising a plurality of storage addresses and a plurality of pre-determined values stored in association with the storage addresses, wherein the pre-determined values are determined according to the mathematical function and the storage addresses at which the pre-determined values are stored;

a matching circuit for matching the input value to a respective one of the storage addresses; and

an output for outputting a respective one of the pre-determined values that corresponds to the respective storage address.

24. The circuit of claim 23, wherein the addresses range from 0 to 255.

25. The circuit of claim 24, wherein the look-up table stores 256 pre-determined values for each of the storage addresses.

26. The circuit of claim 23, wherein the programmable logic device is a field programmable gate array (FPGA).